What is claimed is:

1. A signal amplifier comprising:

a splitter for splitting an input signal into two signals to be transmitted respectively through a first and a second transmission paths;

a first and a second bias control networks for generating base bias signals corresponding to a power level of the input signal by alternating their operation modes, wherein the power level of the input signal lower than a predetermined threshold level is associated with a low input power drive mode and the power level of the input signal higher than the predetermined threshold level is associated with a high input power drive mode of the control networks;

a Doherty amplifier including a carrier amplifier for amplifying the signal transmitted through the first transmission path and a peaking amplifier for amplifying the signal transmitted through the second transmission path; and

a Doherty output network for matching and outputting the signals amplified at the carrier amplifier and the peaking amplifier.

2. The signal amplifier of claim 1, wherein the carrier amplifier reduces idle current in the low input power drive mode and functions as a class AB amplifier in the high input power drive mode in accordance with the bias signal

transmitted from the first bias control network; and

the peaking amplifier is turned off in the low input power drive mode and functions as a class AB amplifier in the high input power drive mode in accordance with the bias signal transmitted from the second bias control network.

3. The signal amplifier of claim 1, wherein the first bias control network includes a V_{contC} pin for receiving different control voltages depending on the power level of the input signal and a V_{refC} pin for transmitting the different base bias signal to the carrier amplifier in accordance with the control voltage fed to the V_{contC} pin; and

the second bias control network includes a V_{contP} pin for receiving different control voltages depending on the power level of the input signal and a V_{refP} pin for transmitting the different base bias signal to the peaking amplifier in accordance with the control voltage fed to the V_{contP} pin.

4. The signal amplifier of claim 3, wherein the control voltages fed to the V_{contC} pin is equal to that of the V_{contP} pin.

5. The signal amplifier of claim 4, wherein the V_{contC} pin and the V_{contP} pin are fed with about 2 ~ 3 V in the low

input power drive mode and about 0 V in the high input power drive mode.

6. The signal amplifier of claim 1, further comprising an attenuator for compensating a gain difference between the first and the second transmission paths in the high input power drive mode, which is located at one of input ends of the carrier amplifier and the peaking amplifier.

7. The signal amplifier of claim 6, wherein the attenuator is implemented by using passive elements or variable gain amplifiers (VGAs).

8. The signal amplifier of claim 1, further comprising a first transmission line for compensating a delay and a phase differences between the first and the second transmission paths.

9. The signal amplifier of claim 8, wherein the first transmission line is implemented by using lumped elements.

10. The signal amplifier of claim 1, wherein the Doherty output network includes:

a second transmission line having characteristic impedance R_{oc} and phase Θ_c, which is arranged at an output end of the carrier amplifier;

a third transmission line having characteristic impedance R_{op} and phase Θ_p, which is arranged at an output end of the peaking amplifier; and

a fourth transmission line having characteristic impedance R_{oc} and phase 90°, which is coupled with the second transmission line.

11. The signal amplifier 10, wherein the second, the third and the fourth transmission lines are implemented by using lumped elements.

12. The signal amplifier of claim 10, wherein the characteristic impedance R_{op} is adjusted in accordance with the formula of $Rop = 50 \cdot (1 + \alpha)$, where α is a size ratio of the peaking amplifier to the carrier amplifier.

13. The signal amplifier of claim 10, wherein the characteristic impedance R_{oc} is adjusted in accordance with the formula of $Roc = 50 \cdot \frac{1 + \alpha}{\alpha}$, where α is a size ratio of the peaking amplifier to the carrier amplifier.